IN THE CLAIMS

Please cancel claims 1-8 and 24-33 without prejudice. Claims 9-23 were previously canceled without prejudice. Please add new claims 34-69. Claims 34-69 are currently pending in the application with entry of this Amendment.

1-33. (Canceled)

34. (New) A computer-assisted model of an integrated circuit comprising:

(a) a bus model;

(b) a plurality of functional block models; and

(c) a plurality of port models, each port model being an unspecified androgynous port model that connects the bus model to a functional block model,

wherein after the bus model is connected to a functional block model, each unspecified androgynous port model is adapted to perform as a target or an initiator of a communication between the bus model and a functional block model.

35. (New) The model of claim 34, wherein each unspecified androgynous port model is dynamically adapted to perform as a target or an initiator.

36. (New) The model of claim 34, wherein an androgynous port model switches between performing as a target and performing as an initiator.

37. (New) The method of claim 36, wherein an androgynous port model is adapted to perform as a target of a first communication and switches to perform as an initiator of a subsequent communication.

38. (New) The model of claim 36, wherein an androgynous port model is adapted to perform as an initiator of a first communication and switches to perform as a target of a subsequent communication.

39. (New) The model of claim 34, wherein each androgynous port model can be adapted to switch between performing as a target and performing as an initiator.

40. (New) The model of claim 39, wherein each androgynous port model is adapted to perform as a target of a first communication and switches to perform as an initiator of a subsequent communication.

41. (New) The model of claim 39, wherein each androgynous port model is adapted to perform as an initiator of a first communication and switches to perform as a target of a subsequent communication.

42. (New) The model of claim 34, wherein each unspecified androgynous model is adapted to perform as a target or an initiator based on the type of interface model that is required for the connection between the bus model and the functional block model.

43. (New) The model of claim 34, wherein each unspecified androgynous port model is adapted to perform as a target or an initiator after the layout of the integrated circuit is finalized.

44. (New) The model of claim 34, a register of an androgynous port model being set to adapt an unspecified androgynous port model to perform as a target or an initiator.

45. (New) The model of claim 34, wherein each unspecified androgynous port model is adapted to perform as a target or as an initiator according to a logic synthesis operation that deletes a state machine configuration that is not used for actual operation of the integrated circuit so that the remaining state machine adapts the androgynous port model to perform as a target or an initiator.

46. (New) The model of claim 34, where each unspecified androgynous port model is adapted to perform as a target or as an initiator according to a logic value of a pin of the interface being set to a "1" or a "0".

47. (New) The model of claim 34, wherein connections between bus model and functional block model minimize a footprint of the integrated circuit.

48. (New) The model of claim 34, wherein each unspecified androgynous port model is adapted to perform as a target or an initiator without adhering to a specification of a component library.

49. (New) The model of claim 34, wherein each unspecified androgynous port model is bi-directional.

50. (New) A method of designing an integrated circuit comprising the steps of:

(a) specifying a communication block for the integrated circuit, including the locations of a plurality of unspecified androgynous interfaces;

(b) identifying functional blocks to comprise the integrated circuit;

(c) positioning functional blocks to form a layout of the integrated circuit so that distances of connections between functional blocks and distances of connections between functional blocks and unspecified androgynous interfaces are minimized; and

(d) adapting each unspecified androgynous interface to perform as a target or as an initiator based on the layout, adapting being performed after functional blocks are positioned to form the layout of the integrated circuit.

51. (New) The method of claim 50, adapting comprising dynamically adapting each unspecified androgynous interface to perform as a target or as an initiator.

52. (New) The model of claim 50, further comprising switching an androgynous interface between performing as a target and performing as an initiator.

53. (New) The method of claim 50, wherein an androgynous interface is adapted to perform as a target of a first communication, further comprising switching the interface from a target to an initiator of a subsequent communication.

54. (New) The method of claim 50, wherein an androgynous interface is adapted to perform as an initiator of a first communication, further comprising switching the interface from an initiator to a target of a subsequent communication.

55. (New) The method of claim 50, further comprising switching each androgynous interface between performing as a target and performing as an initiator.

56. (New) The method of claim 55, wherein each androgynous interface is adapted to perform as a target of a first communication and switch to perform as an initiator of a subsequent communication.

57. (New) The method of claim 55, wherein each androgynous port is adapted to perform as an initiator of a first communication and switches to perform as a target of a subsequent communication.

58. (New) The method of claim 50, wherein each unspecified androgynous interface is adapted to perform as a target or an initiator based on the type of interface that is required.

59. (New) The method of claim 50, wherein each unspecified androgynous interface is adapted to perform as a target or an initiator.

60. (New) The method of claim 50, further comprising finalizing the layout of the integrated circuit.

61. (New) The method of claim 60, wherein each unspecified androgynous interface is adapted to perform as a target or an initiator after the layout of the integrated circuit is finalized.

62. (New) The model of claim 50, adapting comprising setting a register of an androgynous interface so that the interface performs as a target or an initiator.

63. (New) The method of claim 50, adapting comprising performing a logic synthesis that deletes a state machine configuration that is not used for actual operation of the integrated circuit so that the remaining state machine adapts the interface to perform as a target or an initiator.

64. (New) The model of claim 50, adapting comprising adapting each unspecified androgynous interface according to a logic value of a pin of the interface being set to a "1" or a "0".

65. (New) The method of claim 50, wherein positioning functional blocks to form the layout minimizes a footprint of the integrated circuit.

66. (New) The method of claim 50, wherein positioning functional blocks does not account for a type of interface.

67. (New) The method of claim 50, specifying the communication block further comprising specifying a communication block that is part of a foundation block that includes a processor.

68. (New) The model of claim 50, wherein each unspecified androgynous interface is adapted to perform as a target or as an initiator without adhering to a specification of a component library.

69. (New) The model of claim 50, wherein each unspecified androgynous port interface is bi-directional.